# **Wireless Data Acquisition** System (wDAQ)

DESIGN DOCUMENT

Team 19 Client: Avishek Das Advisor: Manojit Pramanik Team Members: Lisa Tordai (Software), Henry Chamberlain (Electrical), Adam Shoberg (Electrical), Vaughn Miller (Computer) Team Email: sddec2419@iastate.edu

Team Website:<https://sddec24-19.sd.ece.iastate.edu/>

# **Executive Summary**

# Development Standards & Practices Used

- IEEE 802.15.1-2002 (Bluetooth)
- IEEE 802.11 (Wi-Fi)
- IEEE 1118.1 1990 (Microcontroller Programming)
- IEEE Citation Format (References)
- ACM Code of Ethics
- Clean Coding Practices
- Surface-Mount PCB Assembly

# **Summary of Requirements**

- Compact Size & Mobility
- Wireless Computer or Mobile Connectivity
- Accurate Data Representation
- Longevity & Reliability
- Ease of Use
- Reasonable Production Cost & Pricing

# Applicable Courses from Iowa State University Curriculum

- EE 2010: Electric Circuits
- EE 2240: Signals and Systems I
- EE 2300: Electronic Circuits and Systems
- EE 3300: Integrated Electronics
- CprE 2880: Embedded Systems I: Introduction
- ABE 271/272: 3D Modeling

# New Skills/Knowledge acquired that was not taught in courses

- Schematic & PCB Design
- Soldering
- Wireless Communication Modules
- LabVIEW Programming

# **Table of Contents**





# List of Figures & Tables

#### **Figures (Images and Diagrams)**

Figure 1: Design Task Decomposition Flowchart *Figure 2: Gantt Chart for Section 3.2 Targets Figure* 3: IkaLogic IkaScope WS200 [1] *Figure 4: Digilent Analog Discovery 3* [2] *Figure* 5: Pokit Pro [3] *Figure 6: Lotus Blossom for Wireless Communication Figure* 7: Input-Output Relationship for an Analog-to-Digital Converter (ADC) [1] Figure 8: Schematic of the Low-Noise Amplifier & Filtering Circuit Figure 9: Schematic of the ADC and Differential Driving Circuit Figure 10: Minimal STM Circuit for Pin-Compatible F4 MCU Figure 11: ESP32 Wi-Fi Module *Figure 12: Block Diagram of the Process Flow (Split into Two Rows) Figure 13: Visual demonstration of how the PAT system operates* [2] *Figures* 14, 15, and 16: Output Waveforms for the Low-Noise Amplifier at Frequencies of 100 kHz, 1 *MHz, and 10 MHz (Left to Right) Figure 17: Plot of Voltage Values Over Time Obtained from Data in LabVIEW* **Tables** Table *1:* Current Monthly Schedule *Table 2: Risks, Severities, and Probabilities*

*Table 3: Personnel Effort Requirements*

Table 4: Public Health, Societal, Environmental, and *Economic Considerations* 

Table 5: Pros and Cons Table Developed Through Market Research

*Table 6: Weighted Decision Matrix*

*Table 7: Similarities and Differences Between IEEE's and NSPE's Codes of Ethics* [7] [8]

*Table 8: Project-Specific Areas of Professional Responsibility*

# <span id="page-5-0"></span>1. Introduction

#### <span id="page-5-1"></span>1.1. PROBLEM STATEMENT

Most modern data acquisition systems, also known as oscilloscopes, require BNC cables to connect to and analyze electrical and physical signals. BNC cables are a type of coaxial cable, which are essentially cords that carry an electrical conductor, surrounded by a protective outer layer, to transmit electrical signals from an electrical circuit or physical body to an external device (i.e., the oscilloscope or data acquisition system) for analysis. In addition to these hefty cables, which are often over two feet long, the data acquisition systems require a corded power supply, and they typically use a built-in graphical display to view signals, as well as physical buttons and knobs to adjust display settings, which take up space and increase the size of the device. The combination of cables, power cords, buttons, and display screens make traditional oscilloscopes and data acquisition systems bulky, heavy devices that are not friendly for mobile data gathering (e.g., attempting to monitor an electrical or physical signal outside of a lab setting) or applications of data acquisition devices within larger systems.

To tackle the size and mobility constraints associated with commercial oscilloscopes, our team wants to create a wireless data acquisition system, powered by a rechargeable battery, that enables mobile real-time data communication using Wi-Fi and is compact enough to fit in about a 1"x5" space. The reason we are striving for mobile capabilities and a small size for our device is because it will be used within a Photoacoustic Tomography (PAT) system in the Biomedical Imaging Laboratory at Iowa State University. A PAT system is a noninvasive device used for biomedical imaging that enables the physical anatomy, oxygen and blood levels, and other biological properties of animals and humans to be identified, like an ultrasound. (ISU's lab will be using the device on small animals.) To accompany the data acquisition device, our team will create a graphical user interface in a software called LabVIEW that enables users to view and analyze data from an external source (e.g., a computer or tablet).

By developing a Wi-Fi connected, battery-powered device that is compatible with external software for data analysis, our team will eliminate the need for BNC cables, power cords, and physical buttons in an oscilloscope and, consequently, be able to easily integrate data acquisition technologies within a larger application.

#### <span id="page-5-2"></span>1.2. INTENDED USERS

Currently, our project's end user is Iowa State University's Biomedical Imaging Laboratory (BILab), which will use the device for medical imaging on small animals. The laboratory users are likely to be fairly skilled with traditional oscilloscopes and quick to pick up on the new technologies. Looking ahead, the goal is for our device to be applied to a larger user base, from research facilities to educational environments. Some of the potential user groups associated with these include Researchers, Lab Assistants, and Educational Institutions, which are described below.

#### **Researchers**

Researchers and scientists will be regular users of our device. These users are highly educated, experienced in a lab setting and with lab equipment, and familiar with data collection and analysis techniques. Their needs include accurate data collection and analysis, mobility and portability of

data analysis within and outside of the lab, and a quick, efficient device. Our device would offer many benefits to the user, such as saving lab space, increasing mobility within and beyond the lab space, and new technology to effectively collect and analyze data.

#### **Lab Assistants**

Our second user group, lab assistants, is another common user; however, their background experience and education may be significantly less than that of a lead researcher. They would need a tool that is easy and relatively fast to learn and become familiar with. Their experience with technology and data analysis may be highly limited, so the device would need to be user-friendly and provide clear, comprehensible data analysis. They would benefit greatly from having an easily accessible tool to help them complete tasks and gather measurements.

#### **Educational Institutions**

This is a device that can be used within educational institutions' research or even lab coursework. These institutions could be colleges, universities, or educational training programs for professionals. Users would need educational tools that facilitate teaching and learning for research practices. They would need live data for students to analyze and comprehend. Our device could provide an affordable solution for educational institutions to provide valuable tools to instructors and students.

<span id="page-6-0"></span>Lastly, see Appendix 1.2 for User Personas, Empathy Maps, and Journey Maps.

# 2. Requirements, Constraints, And Standards

#### <span id="page-6-1"></span>2.1. REQUIREMENTS & CONSTRAINTS

The key requirements for our design include the following: compact size and mobility (constraint), wireless laptop communication, accuracy and reliability of results, and longevity. On the physical side, the device will need to be compact and convenient for mobile applications. The device will initially be used to explore small animals' anatomy and physical makeup & health, as part of a photoacoustic tomography (PAT) system in the ISU Biomedical Imaging Laboratory (BILab), and up to 20 copies of the device will be connected to transducers (devices that convert physical signals to electrical signals) in a circular configuration. Because of the number of devices that will need to fit within the PAT system, the size of the devices is constrained to an approximately  $1$ " by  $1$ " by  $5$ " volume. Furthermore, since the devices will be rotating and moving continuously, they will also need to be wireless to prevent cord entanglement.

In the way of the user interface and experience, we will need the device to be Wi-Fi connected to enable wireless communication with the user interface and control software on a computer or mobile device, as well as be easy to use. The wireless connection requirement also ties into the physical constraints of the device because there will not be space on the PAT system for the traditional features of an oscilloscope. Most scopes contain a graphical display with buttons to view and analyze signals, but with our device's application, having a display on each individual scope would be redundant, and there is no way that the buttons and display would be able to fit in a 1" by 5" space. It makes much more sense to have a single software program where the user can

view and adjust signals from all scopes (up to 20) at once, which can be best achieved by wirelessly connecting the scopes to the software program, so this is one of the key requirements. For ease of use, we want to make sure the device is easily accessible to all, which means creating a product that can be used by lab technicians and amateur users alike. We will want the user interface to be straightforward and easy to use, as well as ensure the device can easily be connected physically to the PAT system and wirelessly to the user software. This way, newer lab employees and nontechnical users will all be able to utilize our product.

The main functional requirement of our device is to obtain accurate and reliable results. This requirement is somewhat vague and difficult to quantify because there is always a possibility of error in results, even if the results are consistent between devices and trials. One way we can more easily gauge the accuracy and reliability of our device is by ensuring we are meeting the specifications in the project proposal. We have slightly modified the requirements, but we are looking to create an RF (MHz frequency range) signal with an amplitude of  $1$  V (peak-to-peak) and a rise time in the range of around  $\frac{1}{5}$  µs. Additionally, we are looking for an ADC with a 12-bit resolution and a sampling rate of at least 100 MS/s (million samples per second). For transmission to the user interface, we want to have a data rate of over 100 Mbps (megabits per second) to ensure fast transmission of results. By creating a device that meets all or most of these specifications, we will be much more likely to have a product that gathers and transmits data accurately and consistently.

The last major requirement for our device, longevity, ties into economic and environmental applications, as well as resource requirements. We will want the device to be durable and long-lasting, because it will be duplicated up to 20 times and used in a larger application for data acquisition. If the device we create breaks easily or becomes less reliable over time, we may need to recreate a higher quality product, which will cost us time, money, and resources, and delay the use of the PAT system until the DAQ systems can be fixed. Also, we would waste significant resources and discard old products, which would have an environmental cost. By creating a quality product from the start that is likely to last for several years, we can avoid complications in the long term.

#### <span id="page-7-0"></span>2.2. ENGINEERING STANDARDS

**IEEE Microcontroller Programming Standard (IEEE 1118.1 1990):** This will likely be used because a major portion of the project is programming the microcontroller to receive the digitized data and perform an action. So, it can be assumed that programmers will need to use this to standardize code and be as efficient with distributed data acquisition.

**IEEE Wi-Fi Protocol (IEEE 802.11):** Our project will use an ESP32 chip that will send data via Wi-Fi to a computer. This device makes use of 802.11 for setting up local area networks and MACs.

# <span id="page-7-1"></span>3 Project Plan

#### <span id="page-7-2"></span>3.1 PROJECT MANAGEMENT/TRACKING PROCEDURES

Our team has adopted an agile project management style. We are trying to complete tasks and milestones for our project in a timely manner to satisfy our client's expectations but are not

restricted to a firm timeline. Our client would like the project to be completed a couple of months ahead of the December deadline, because he is hoping to publish an academic paper with us about our project after it is completed. We are currently meeting weekly with our client to discuss our progress, ask questions, and formulate tasks and deliverables for the project as we go, so our timeline is flexible and adaptive to new ideas and design changes. We typically complete design tasks relatively quickly and delegate electrical and software/computer portions of the design to the respective team members.

This project management style has worked well for our team so far, because with the wireless data acquisition system we are designing, many of the software and computer-related portions of the device (e.g., Wi-Fi communication, user interface, microcontroller and analog-todigital converter) can be designed independently of the electrical parts of the device  $(e.g., the$ amplifier, signal filtering and processing, and battery power supply), which makes it more practical to split up most tasks, while working together as a team to bring the components of the device together in the top-level design. Additionally, some tasks and design sprints end up taking significantly more or less time than originally anticipated, making it more sensible to adapt to new timelines as needed. Lastly, our client likes to be closely involved with our work and communicate with us regularly, as well as alter the design and timeline for the project occasionally, which makes the agile working style a much more logical choice overall.

In terms of tracking progress, most of our communication and progress updates within our team and client occur through a shared Microsoft Teams channel. We use our Teams channel to communicate regarding weekly meetings and progress, ask questions, and post updates, documents, and deliverables. These posts include weekly progress report PowerPoints, Schematic documents and PCB files, and code files for software items, posted under the "Files" section of our Teams channel. Eventually, most of these deliverables will also be shared on our team website. Aside from Teams, our team has a Snapchat group chat for casual communication, and we use Outlook and Zoom for communication with our faculty advisor. We have been able to work successfully so far without using Git, Trello, Slack, and related project management tools, but we may end up using these to some extent in the future.

#### <span id="page-8-0"></span>3.2 TASK DECOMPOSITION

Even though we are using mainly an agile project management style, our project can be split into three major "targets": project planning and design, prototyping, and building the final product. As for specific tasks that must be completed to create the wDAQ device, we need to amplify and filter analog signals (physical signals from test subjects), digitize the signals, send the signals to a computer software user program via Wi-Fi, and display the signals to the user interface. *Figure* 1 below shows the design plan and flow that our team created using Figma.



Figure 1: Design Task Decomposition Flowchart

Our team will reference this flowchart throughout the year for a high-level overview of the requirements and deliverables we want to create, but on a smaller scale, we can divide the major

phases and targets of the project into smaller tasks. The list below describes the subtasks for each target associated with our design.

#### **Target I: Project Planning and Design**

- Understand the requirements and needs of the client and users
- Gather inspiration and ideas by exploring related products on the market
- Create a flexible initial plan of work
- Break the design steps from the flowchart into smaller milestones and tasks
- Delegate individual tasks and responsibilities to team members on a weekly basis
- Design the device in small steps or "sprints"

#### **Target II: Prototyping**

- Order parts and electrical components to create a prototype PCB for the device
- Solder PCBs for individual components of the device and connect them with header pins
- Test the PCB to ensure proper electrical connections and functionality
- Develop user software to a functional level and connect software with the device
- Observe and analyze the results of the prototype
- Discuss shortcomings, design errors, and areas of improvement

#### **Target III: Final Buildout**

- Host an evaluation & feedback session with the client and users of the product
- Analyze user and client feedback to recognize key areas of improvement
- Brainstorm and make decisions as a team on changes needed for the final product
- Gather new materials or parts for the device as needed
- Work out software bugs and ensure the program is working up to a high standard
- Rebuild the device or parts of the device as needed to meet requirements
- Test the final product and ensure accuracy and satisfaction of requirements

As mentioned in the previous section, many aspects of the project will be delegated specifically to electrical, computer, or software team members, as this will enable team members to work in the areas where they are the most comfortable and skilled. Creating a schematic and PCB for the amplification and filtering stages of the circuit, as well as the battery and battery protection system for the power supply, and parts of the analog-to-digital converter (ADC) will be assigned to electrical team members, while the design and testing of the microcontroller and parts of the ADC circuit will be assigned to the computer and software members, and the design of the user interface and Wi-Fi connection will be almost entirely the responsibility of the software team member. When building the device and combining individual parts, all four team members will come together to ensure the device meets all requirements.

#### <span id="page-9-0"></span>3.3 PROJECT PROPOSED MILESTONES, METRICS, AND EVALUATION CRITERIA

The milestones, metrics, and performance targets we will be aiming toward with our project are listed below. We separated these targets by steps from our initial design plan because this plan has more concrete metrics and objectives than the "targets" plan from above. Our client will be designing the battery, so we do not have milestones or metrics for this currently.

## **Amplifying and Filtering the Input Signal:**

- Milestone A1: The amplifier has a Bandwidth of 100 kHz  $\sim$  1 GHz
- Milestone A2: System Gain of up to 60 dB with low signal degradation
	- o Milestone A2.1: The amplifiers produce 2 dB of noise at 300 MHz
- Milestone A3: The system draws a current of  $70$  mA or less (corresponding to a power draw of  $864$  mW or less with a 12 V power supply)
- Milestone A4: The system has an input impedance of 50  $\Omega$ 
	- o Milestone A4.1: The amplifier is connected by SMA cables with impedance of 50  $\Omega$
- Milestone A5: The PCB contains two single-rail IC amplifiers (cascaded together)
	- $\circ$  Milestone A5.1: The IC amplifiers are powered by a single 12 V DC supply
	- o Cascading of amplifiers will occur later when building the full device's circuit

## **Digitizing the Amplified Signal:**

- Milestone B1: Suitable ADC has 12 Bits of resolution with sampling rate of 120 M samples/sec to avoid the effects of aliasing
- Milestone B2: The ADC takes differential (positive and negative) signal inputs.
	- o Milestone B2.1: Differential inputs are sourced from the output signals of the LNA
- Milestone  $B_3$ : The ADC is supplied by 5 volts, fed from our single 12 V DC supply.
	- $\circ$  Milestone B3.1: The ADC supply voltage is adjusted to 5 V using a voltage regulator such as the LM7805 from TI (implemented in ADC driving circuit).

# **Wirelessly Sending Digital Signals to Computer:**

- Milestone C1: Obtain communication module parts compatible with our project's needs
	- $\circ$  Milestone C1.1: Research and choose one Bluetooth and one Wi-Fi device that fit the needs of our project
- Milestone C2: Testing capabilities of Bluetooth vs. WIFI
	- o Milestone C2.1: Using Arduino to program Bluetooth module to successfully send and receive data from laptop
	- o Milestone C2.2: Using ESP32 to program Wi-Fi module to successfully send and receive data from laptop
- Milestone C3: Programming device to send data over server for LabVIEW to be able to receive data

• Milestone  $C_4$ : Program project microcontroller to send data through the Wi-Fi Module

#### Logging and Displaying Data in User Interface:

- Milestone D1: Discover capabilities of LabVIEW tools to connect with Bluetooth and Wi-Fi
- Milestone D2: Create LabVIEW VI to create a connection with Wi-Fi Module
- Milestone D3: LabVIEW reads in data from LabVIEW server
	- o Milestone D3.1: Read in values from Wi-Fi Module
	- $\circ$  Milestone D3.2: Display data in a graph for the user to be able to analyze
- Milestone D3.3: Allow user to log and export data

# <span id="page-11-0"></span>3.4 PROJECT TIMELINE/SCHEDULE

The timeline for our project does not line up with the proposed calendar for projects given in  $EE/CprE/SE/CybE$  491, because our client is pushing us to jump ahead of the recommended schedule and complete the planning & designing quickly, reserving the remaining time in the Spring & Fall for prototyping, revising, building and implementing the final device, and writing an academic paper about the project. This is quite a bit different from the suggested calendar, which recommends using the entire spring semester for designing, planning, and research, and completing the entire implementation and buildout of the project in the Fall semester.

The simplified Gantt chart for our project, split into our three main "targets" described in Section 3.2, is shown below in *Figure* 2. Please note the January work begins January 23; May work ends May 10; August work begins August 26; and December work ends December 13.



*Figure 2: Gantt Chart for Section 3.2 Targets*

A more detailed monthly schedule for our project that elaborates upon and follows the targets and dates from the Gantt chart is given in *Table 1* below. The schedule also incorporates the estimated completion dates of specific milestones and metrics from Section 3.3. The tasks and objectives for January through March are finished, but they are included for reference.







## Table 1: Current Monthly Schedule

This schedule incorporates the estimated timelines for work and completion of each of our three main "targets", as well as for each of the milestones given in Section 3.3. Although the schedule mentions presenting our project to industry and faculty panels, writing our final design document, and creating & publishing an academic paper on our project, we chose not to classify these as specific targets or milestones, because they are technically not part of our actual project, and we are unsure whether or not we will decide to publish an academic paper.

## <span id="page-14-0"></span>3.5 RISKS AND RISK MANAGEMENT/MITIGATION

The potential risks associated with each task or "sprint" of our project are given in *Table 2* below, with a severity level and estimated probability assigned to each risk. For risks classified with "high" severity or an estimated probability greater than 0.5, a risk mitigation plan is also given beneath the table.





*Table 2: Risks, Severities, and Probabilities*

The list below describes the risk mitigation strategies for the risks from the table with high severity or probability above  $0.5$ , which are referenced by  $(1)$ ,  $(2)$ , etc. in the table.

- 1. System gain is less than expected: The first risk is that the system does not have enough gain to amplify the signal to the required magnitude of the ADC. We have discussed steps to add female header pins so we can add more IC modules in the future to give the system more dynamic and user selected functionality. This would in turn address any problems with system gain.
- 2. Having latency in data from machine to GUI: The device is only useful if the user can see real-time data as a regular oscilloscope would provide. We will need to send over the server a large quantity of data continuously, so we must ensure that the Wi-Fi module we use is capable of this. We also need to ensure the interface we program in LabVIEW will process the data and display it as efficiently as possible.
- 3. Having an unstable connection with the Wi-Fi module: One migration strategy we have currently enacted is the use of high-end Wi-Fi modules that allow for stable connection within a 20-foot radius. Given the condition this device will operate under, it can be assumed that it will give us the needed stability for consistent connection.
- 4. Some components ordered have incorrect nominal values, tolerances, etc.: This is a common mistake when ordering parts that can easily be fixed by verifying the correct values, component properties, etc. with the circuit schematic and placing another order with the corrected parts.
- 5. Specific components or parts are out of stock: Typically, having parts in a design or order that are out of stock can be fixed or worked around easily by substituting parts or components with similar values and characteristics, ordering from another supplier, or purchasing an identical or similar component from a different manufacturer.
- 6. Wi-Fi module is not compatible to communicate between microprocessor and GUI: Proper research using online documentation and product help services will be conducted before the purchase of the device to ensure its compatibility with all components.
- 7. GUI missing necessary data and functionality of the user: The product's main purpose is to serve the user with important information and data analysis. We need to ensure that we are producing the needs of the user in the GUI and that it is easy to collect data.
- 8. Battery protection system doesn't properly protect from overcurrent/overheating: Our client will be handling most issues related to the battery and battery protection system. If the battery is not properly protected from overcurrent or overheating, the consequences could be severe, such as the battery catching fire or exploding. One way these risks could be mitigated is through the use of a voltage regulator in the battery pack (such as the  $TI$  $LM<sub>7805</sub>$ ) that keeps the voltage within a safe operating range at all times.
- 9. Full design doesn't fit on PCB (front & back): If this problem becomes apparent, we will have strategies to remove redundant components and switch footprint sizes of devices.
- 10. Device doesn't fit in the PAT System: To mitigate the risk that the overall device doesn't fit in the designated brackets, we have sectionalized the design into phases and parts while selecting the smallest components that do not reduce overall performance. We have also taken steps to reduce the use of redundant components that were not crucial to the system's performance.

#### <span id="page-16-0"></span>3.6 PERSONNEL EFFORT REQUIREMENTS



Personnel effort requirements are given in *Table* 3 below.





*Table 3: Personnel Effort Requirements*

The table above is an estimate for the total number of person-hours that will be required for this project. The table does not include 491 class time, because this time is not considered "hours" where the team is working on the project. However, it does incorporate the time that will be spent outside of class working on presentations and design documents for the course, as well as preparing an academic paper and presentations for our client, meeting with our client and faculty advisor, implementing our device after it is completed, and other tasks and requirements that fall outside of the targets, milestones, and metrics given for the project. Tasks corresponding to the three targets are bolded in the table and milestones are included within these tasks (see schedule from Section 3.4 for explanation of where milestones and metrics fall within each task).

Since our team members have agreed that we do not want to spend more than 10 hours per week on average working on Senior Design, the total available time for each member should be no more than 290 hours (since there will be 29 "working" weeks across the two semesters). As the table shows, the projected hours per member is within this limit, with most members expecting to spend an average of about 7.5 hours per week working on the project.

#### <span id="page-18-0"></span>**3.7 OTHER RESOURCE REQUIREMENTS**

Aside from the obvious financial resources that will be required to fund our project, we will require tools and equipment, parts and materials, training and instruction, and some amount of labor. A breakdown of our needs associated with each of these resources is given below.

#### **Tools and Equipment:**

- o Soldering equipment (iron, tin, desoldering wick, flux, wire cutters, clamp)
- $\circ$  Personal protective equipment (safety goggles and gloves for soldering)
- o Electrical measuring tools & lab equipment (multimeter, oscilloscope, etc.)
- o Software (Arduino IDE, LabVIEW, MATLAB, EasyEDA, NI Multisim, etc.)
- $\circ$  3D Printer & 3D modeling software

## **Parts and Materials:**

- o Resistors, capacitors, and inductors (surface-mount and through-hole)
- o Miscellaneous surface-mount and through-hole components
- o STM32 Microcontroller IC
- o ESP Wi-Fi Module
- o Analog-to-Digital Converter (ADC) IC
- o Amplifier ICs (Aside from RF Amplifier)
- o Arduino Board
- o Printed Circuit Boards (PCBs)
- o Breadboards
- o Jumper Wires
- o SMA Cables
- o RF connectors

# • Training and Instruction:

- o EasyEDA and NI Multisim (circuit simulation & design software) tutorials
- o LabVIEW training and assistance (as needed)
- o Soldering training (as needed)
- o General electrical/software questions for client
- **Labor:**
	- o ETG Parts Orders
	- o PCB soldering & assembly (from ETG or JLCPCB)
- o Programming microcontroller and LabVIEW
- o 3D printing case for assembly

# <span id="page-20-0"></span>4 Design

## <span id="page-20-2"></span><span id="page-20-1"></span>4.1 DESIGN CONTEXT

## 4.1.1 Broader Context

Our design problem is currently situated in the relatively limited context of the Biomedical Imaging Laboratory (BILab) at Iowa State University, so lab technicians and research associates will be the main users and parties affected by our design in the immediate future. Looking further ahead, however, we may expand the implementation of our project to different user groups, which would entail a better understanding of the needs of all user parties associated with our product.

The public health, societal, environmental, and economic considerations for our project are given in *Table 4* below.



	acquisition of materials, such as over- purchasing and wasting unused materials.	items we need when we need them will yield a higher degree of overall sustainability.
Economic	Our project is financially viable for our team because most of it is funded through Iowa State University Engineering resources (e.g., ETG). The eventual cost to consumers will depend on the final cost to build the product, along with the device's reproducibility and economies of scale. Once completed, our design may have a considerable impact on the university's financial resources.	The relatively high development cost of our product may create negative financial consequences for the university's engineering departments, which will be funding the bulk of our project, mainly due to the frequent need for parts and materials to build and test prototypes of our device, which we often order in excess supply and sometimes end up scrapping when our design iterations are flawed.

Table 4: Public Health, Societal, Environmental, and *Economic Considerations* 

# <span id="page-21-0"></span>4.1.2 Prior Work/Solutions

The background review for our project consisted mainly of market research into products that currently exist which provide similar features or functionality to the device we are striving to procure. We looked at the solutions these companies created, how they related to or differed from our design, and what the advantages or shortcomings of each product and company were. The three similar companies and products we researched are described in detail below.

## **IkaLogic: IkaScope WS200 [1]**

The IkaScope WS200 is a data acquisition tool that connects wirelessly to computers (using Wi-Fi) to display signals. Its battery lasts up to a week between charges, it offers relatively similar specifications and performance characteristics to our design at a comparable size, and it is priced at approximately \$250. The manufacturer, IkaLogic, partners with major distributors, such as DigiKey and Mouser, to distribute its products; however, the small size of the company (under ten employees) significantly limits the scope and scale of its operations. *Figure* 3 below shows an image of the IkaScope WS200.





# **Digilent:** Analog Discovery 3 [2]

The Digilent Analog Discovery  $3$  is a data acquisition system that connects to computers or similar devices using a USB Type-C connection. It is currently used by multiple ECpE labs at ISU, mainly due to its compatibility with multiple types of software, including MATLAB, LabVIEW, and NI WaveForms. In addition to data acquisition & Analysis, the DAD can also be used in combination with the WaveForms app to function as a signal generator. Digilent, the manufacturer of the DAD, is a division of National Instruments (NI), which is a large multinational software & hardware corporation, so the company certainly has a leg up in terms of production, product availability, and reputation. Additionally, almost all Digilent devices are compatible with a wide range of new and existing technologies and software tools, and the company offers special discounts to academic user groups, which could make it an advantageous option for universities and research labs to consider. The only major downside to Digilent is the lack of completely wireless connection to its data acquisition devices, as they still require a USB-C connection to computers or other devices for analysis. *Figure* 4 below shows an image of the Digilent Analog Discovery 3.



*Figure 4: Digilent Analog Discovery* 3 [2]

# **Pokit:** Pokit Pro [3]

The final company our group researched was Pokit and its wireless data acquisition tool, Pokit Pro. The Pokit Pro utilizes Bluetooth to connect wirelessly to software (rather than Wi-Fi) and it is powered by a USB-C rechargeable battery, as our design is striving to implement for its power supply. The ADC sampling rate and input signal specifications are also quite like our design. One major disadvantage of the Pokit Pro in the context of our application is the fact that it limits signals to a bandwidth of 200 kHz, making it essentially useless for high-frequency (RF) applications like ours. Another disadvantage is simply the use of Bluetooth for data transfer instead of Wi-Fi, because data transfer is generally much slower with Bluetooth than Wi-Fi (sometimes less than ten percent of the data transfer rate), so there will be considerable latency with data transmission for this device compared to our design. As for the manufacturer, Pokit offers numerous other data acquisition and related electrical hardware products for sale, including another data analysis device that is even more compact than Pokit Pro (at the cost of more limited user features), but their devices are not widely available and are somewhat pricey. *Figure* 5 below shows an image of the Pokit Pro.



*Figure 5: Pokit Pro [3]*

*Table* 5 below provides a list of pros and cons of our team's solution compared to those of two related product categories on the market: traditional oscilloscopes and existing wireless/mobile data acquisition devices (we chose the Digilent Analog Discovery 2 as our metric for analysis).

	<b>Alternative 1: Traditional</b> Oscilloscope	<b>Alternative 2: Digilent Analog</b> Discovery 2	<b>Alternative 3: Our Design</b>
<b>Pros</b>	- Highly accurate - Data sent in real time - Wide bandwidth - Can read most signals - Safe to operate - Support functions like math - Established documentation	- Compatibility with multiple types of software - NI WaveForms app - Many functionalities and capabilities for data analysis	- Precise high-frequency data - Portable and user-friendly - Small size - Minimizes use of equipment - Likely very inexpensive compared to similar market options
<b>Cons</b>	- Fairly costly to acquire outside of a university setting - Bulky device - Requires technical training or exposure to the device - Requires tuning - Uses probes (hardwired connection) - Requires corded power connection	- Requires USB-C for power supply and software connection (not fully wireless) - Larger size than our device	- Small footprint comes at the cost of lower battery capacity and potentially inferior performance - Not as fast as high-end portable oscilloscopes - No established brand reputation or marketplace presence - No customer support or professionally evaluated documentation

Table 5: Pros and Cons Table Developed Through Market Research

# <span id="page-23-0"></span>4.1.3 Technical Complexity

In the way of internal technical complexity, our design incorporates six interconnected components: a transducer, low-noise amplifier, analog-to-digital converter (ADC), microcontroller, Wi-Fi module  $\&$  connection, and graphical user interface (GUI), each of which leverage a combination of electrical, computer, and software engineering principles. The amplifier manipulates analog signals, using passive components and integrated circuits (ICs) to amplify them; the ADC circuit, which has a specific bit resolution and sampling rate that must be considered in relation to other parts of the design, uses IC amplifiers and passive components to convert the single-ended signal to a differential (double-ended) one, as well as incorporates a linear voltage regulator and DC-DC buck converter that steps down the power supply voltage; the microcontroller and Wi-Fi modules are Systems-on-Chip that are biased and controlled by a larger circuit; the Wi-Fi module transmits data from the microcontroller to the GUI at a fast data transfer rate, and is tested on a breadboard using an Arduino evaluation board; and the GUI, being written in LabVIEW software and connected to the device with Wi-Fi, makes use of primarily software and computer engineering principles in its design & implementation.

On the external side of technical complexity, numerous aspects of our device match or surpass cutting-edge technology in the industry. For one, the use of a rechargeable battery to power an oscilloscope is a novelty, as only a few other devices on the market utilize a rechargeable battery rather than a corded power supply. Next, the compact size of our device beats the size of most oscilloscopes on the market: it will occupy an approximately  $1''$  by  $5''$  by  $1''$  space, making it much smaller than traditional box oscilloscopes. Next, the use of Wi-Fi to communicate data makes our device one of the fastest in industry, with a data transfer at a rate of up to 150 Mbps (megabits per second), much faster than wireless DAQ systems that utilize Bluetooth communication, which are limited to a data transfer rate closer to 10-20 Mbps. Lastly, the ability to directly "probe" real-world physical signals is a cutting-edge technology: using an SMA connection, our device is directly compatible with transducers, which quickly translate physical signals to electrical signals.

#### <span id="page-24-0"></span>4.2 DESIGN EXPLORATION

#### <span id="page-24-1"></span>4.2.1 Design Decisions

- **Two-stage, single supply voltage low-noise RF amplifier:** Per the decision specifications, the device needs to amplify an input signal from  $\text{imV}$  to 1 volt. This required two amplifier ICs, MAR-6SM+, to be cascaded together to achieve the gain required. The device also needs to be biased by a single voltage supply to minimize complexity and size.
- High-speed Microcontroller Unit and separate ADC: Due to the bandwidth requirement, the sample rate of the device needs to be at least 15 million samples per second or higher. An FPGA and ADC would be the best choice if time and money weren't a concern, but a microcontroller-based solution is more familiar and far less expensive, and modern offerings from ST Microelectronics are capable of handling data processing at high speed. The ADC also needs to be as noise free as possible at the frequencies we're working with, so we've chosen to employ a separate ADC IC in series with an STM32 MCU.
- Wireless connection of device to user software: We have decided to go with a Wi-Fi connection (instead of Bluetooth) because Wi-Fi chips allow more data to be transmitted. This allowed the team to narrow down the research of a suitable module. The module of choice ended up being the  $ESP_32$  due to its ease of use, low cost, performance matching, and compatibility with other technologies being used in the project.
- **EasyEDA for PCB Design:** One of the major components of this project is the design of our own PCBs. In the end, we decided to go with EasyEDA for a multitude of reasons, the first being its large library of parts. This minimizes the need for third-party websites to import footprints and other files. The second reason for choosing EasyEDA was its file sharing capabilities. The program allows for team folders, where members can work remotely on the same file. This maximized team collaboration and saved man hours. The last reason EasyEDA was selected for the PCB design was because it was easy to buy the components and PCB directly from the program.
- Rechargeable battery power supply: We will be utilizing a rechargeable battery to power our device alongside a battery management system to protect the battery from overcurrent, designed partially by our student team and partially by our client. The battery choice comes down to three potential options: Lithium-ion, Nickel Cadmium (NiCd), and Nickel-Metal Hydride (NIMH), all of which are compact and can be compatible with integrated USB Type-C charging. We will either be designing the battery management system (BMS) or using a preassembled chip, but a study on the power usage of the circuit and power management optimization, which will be completed after designing a prototype of the device (without the battery), will enable us to determine the requirements of the battery and associated BMS. We will also be implementing a voltage regulator (such as TI's

 $LM<sub>7805</sub> Linear RegularIC (with the battery's power supply that will ensure we supply$ steady DC voltages to the circuits within our design and avoid accidental overcurrent.

#### <span id="page-25-0"></span>4.2.2 Ideation

For each of the key design decisions, our team created a Lotus Blossom Diagram to identify potential options and solutions. The wireless communication aspect of the design process was one of the few areas where our team had more leniency and "options" to choose from in the design, rather than needing to use a specific technology or device to achieve a requirement. The section of the Lotus Blossom Diagram where we identified possible options and design considerations relating to wireless communication is shown in *Figure* 6 *below*.

Option 1: Bluetooth	Option 2: Wi-Fi	Data transfer rate (faster = better)
Connection range (only need a few meters)	н Wireless Communication	Connectivity to laptop (easier = better)
Cost of technology		

*Figure 6: Lotus Blossom for Wireless Communication*

The options, constraints, and considerations our team came up with for wireless communication using the Lotus Blossom technique are described in detail below.

- **Bluetooth (Option 1):** Bluetooth communication chips have relatively high latencies for wireless communication  $(30+ms)$  and somewhat slow data transfer rates (typically no more than 30 Mbps (megabits per second)). The connection range is also small (typically 10-20 meters or less). The advantages of Bluetooth include mostly reliable & consistent connectivity and secure data transfer.
- Wi-Fi (Option 2): Wi-Fi communication tends to have a lower latency for wireless communication (often less than 10 ms) and a much higher data transfer rate than Bluetooth (over 100 Mbps), which enables high-speed data collection at all times. The connection range of Wi-Fi chips is also significantly higher than BT chips  $(\sim$ 100 meters). Wi-Fi connection is also usually consistent and is highly secure.
- Data Transfer Rate: The data transfer rate of the device is an important factor in the decision for wireless communication because a high data transfer rate ensures fast communication with software and compatibility with the sampling rate of the ADC and clock speed of the MCU. Our ADC of choice (ADC12020 from Texas Instruments) has a sampling rate of at least 20 MS/s (million samples per second), and the MCU (microcontroller) has a clock speed of over 100 MHz, so the technology we use will need a data transfer rate that matches or surpasses these rates to ensure compatibility. This makes Wi-Fi a much more attractive choice already.
- **Connection Range:** The connection range of our wireless communication is not important, because the user will most likely be using the LabVIEW software close to the device (i.e., within a few meters). However, having more flexibility with the distance between the user and the device is always a plus. Wi-Fi chips offer a connection range in excess of 100 meters, while most Bluetooth chips are limited to a connection range of a few (up to 10) meters, which makes Wi-Fi a better option again.
- **Ease of Laptop Connectivity:** Both technologies are relatively easy to connect to once they have been properly configured. Initial tests of both technologies have shown some connection difficulties and delays, but they typically resolve quickly. From a user perspective, Wi-Fi networks are generally a bit easier and faster to connect with than Bluetooth devices, and the use of a security key makes them a safer data transfer choice.
- Cost of Technology: Most marketplace Bluetooth and Wi-Fi chips are relatively inexpensive (in the range of  $$10$  to  $$20$ ), so there is not a significant discrepancy between the costs of the two technologies, which makes this an unimportant factor in the decision process.

# <span id="page-26-0"></span>4.2.3 Decision-Making and Trade-Off

For the decision-making and ideation process, our team used a weighted decision matrix to identify the pros and cons of each of the potential options for wireless communications (See Table 4 below). We selected this option for ideation because it enables us to easily understand the different advantages, disadvantages, and characteristics of Wi-Fi and Bluetooth technology, as well as make more direct comparisons between the two technologies to make a well-informed decision. The process of a weighted decision matrix involves identifying the relevant considerations and factors associated with our two options, assigning a "weight" (importance factor) from  $1$  to  $5$  for each factor, and assigning a performance score for each technology and consideration, also from  $1$  to  $5$ , with an explanation of how well each technology satisfies each of the criteria.





#### *Table 6: Weighted Decision Matrix*

Note: Based on the weighted matrix, *Table 1*, it is evident that the use of a Wi-Fi chip is the way to go for our project. It scored significantly higher in the most heavily weighted factor, data transfer rate, while staying on par with Bluetooth for every other factor.

#### <span id="page-27-0"></span>4.3 PROPOSED DESIGN

#### <span id="page-27-1"></span>4.3.1 Overview

A high-level view of our design is a low-cost, user-friendly, wireless oscilloscope (tool used for viewing properties of signals). The design starts off with a low-strength, high-frequency signal being captured and sent to an amplification and filtration stage. The amplification stage essentially takes this initial signal and scales it by a factor of close to 1000. The purpose of the filtration stage is to remove unwanted components of the signal. Like how a coffee filter works, it removes the unwanted portions of the signal (the "coffee grounds") and passes the portions we do want (the coffee). Following this, the filtered and strengthened signal travels to the analog-to-digital conversion stage. This portion of the device uses components that essentially follow the original signal, but in the form of steps (like staircases). Reference *Figure*  $\tau$  below for a visual representation of the input-output relationship for an ADC.



*Figure* 7: *Input-Output Relationship for an Analog-to-Digital Converter (ADC)* [1]

Once the signal has been digitized, computers can perform actions with the signal. Following the signal's digitization, it travels to a component called a microcontroller. This is the jack of all trades for electronics components. It can perform actions based on user-determined instructions using a component called a central processing unit (CPU). It also has storage space to hold onto information pertaining to the digitized signal. Once the microcontroller has executed its user instructions, it spits the information out of the output pins. The last stage of hardware the information travels to is the Wi-Fi module. Like how you connect to your Wi-Fi at home, a user can connect to the Wi-Fi module on their computer. This is where the information is transferred wirelessly to the computer for the user to see on their computer or mobile device.

# <span id="page-28-0"></span>4.3.2 Detailed Design and Visual $(s)$

The design of our device consists of six different interconnected stages that operate in close succession (the first of which is technically not part of the device). A technical description of each of these stages, followed by a block diagram showing images of the individual components and the order of their connections, are given below.

- **Stage 1: Photoacoustic Transducer:** A Photoacoustic Transducer will provide the input signal to each DAQ system that is implemented within the Photoacoustic Tomography (PAT) system, connected by male and female SMA ports. These transducers take physical signals from the real world (in our application, sound waves and echoes from animals) and transmit them to the DAQ devices as electrical signals that can be operated on and analyzed. The transducers have already been designed and implemented within the PAT system, so our team will only be concerned with connecting them to our devices.
- **Stage 2: Low-Noise RF Amplifier & Filter:** The low-noise amplifier takes a 1 mV (peak-topeak) analog input signal and amplifies it to an amplitude of approximately  $1$  V (peak-topeak). Thus, the overall amplifier has a gain of close to 1000 V/V, or 60 dB on a logarithmic scale, which is implemented by cascading two amplifiers with individual gains of approximately 32 V/V (30 dB). We chose the  $MAR\text{-}6SM\text{+}$  amplifier by Mini Circuits for our design. The amplifier is considered "low-noise" because it does not distort the output signal or significantly degrade the signal-to-noise ratio: the noise figure of the amplifier is  $2$ dB at 300 MHz. Another important characteristic of the amplifier circuit is wide bandwidth: because we want to amplify radio frequency signals per the project proposal, we will require an amplifier bandwidth in the MHz range, which the MAR-6SM+ amplifier offers (with a wideband frequency range from DC to 2 GHz). The operating bandwidth of

our overall amplifier circuit is limited to the range of 100 kHz to 2 GHz through a simple RC network and current-limiting inductor at each amplifier's output. The other notable features of the amplification & filtration circuit are: a 50  $\Omega$  input impedance (which determines the necessary impedance of the signal output by the transducer); a current draw of at most 70 mA corresponding to a power dissipation of at most  $864$  mW across the circuit (achieved after the complete prototype of the device with a power management & optimization study); and lastly, a single-rail  $12$  V DC power supply, which will ultimately be sourced from the battery and fed through a voltage regulator (LM7805 from Texas Instruments) to ensure consistent voltage. *Figure 8 below shows the complete schematic for the low-noise amplifier. From left to right, the schematic shows the RF input (through an* SMA port), the two MAR-6SM+ amplifiers cascaded together (rectangular symbols), the RLC *biasing networks used to control the gain and bandwidth of the amplifier, and the RF output* (input to the ADC circuit). The small box with arrows coming out of it on the upper left shows the pins for the 12 V DC supply and the common ground.



Figure 8: Schematic of the Low-Noise Amplifier & Filtering Circuit

• **Stage 3: Analog-to-Digital Converter (ADC):** The ADC circuit converts our amplified analog signal to a digital signal, i.e., a signal that takes on only discrete amplitude values (like a square wave) rather than a continuous spectrum (like a sine wave). The ADC chip we are using, the  $TI$  ADC12020, has 12 bits of resolution and operates at a sampling rate of 20 MS/s (million samples per second) or more using an internal sample-and-hold circuit to minimize power consumption. The circuit utilizes a differential pipeline architecture, so it takes both a positive and negative-ended analog input for digitization. The differential inputs are produced from the output signal of the low-noise amplifier circuit through the use of a differential driving circuit that incorporates an instrumentation amplifier, a general-purpose op amp, a separate power supply circuit containing a precision bandgap shunt voltage reference (used to reduce the voltage from 12 V to  $5$  V DC (note that the LM7805 IC from Texas Instruments may be used in place of this voltage reference), and a multitude of resistors and capacitors that maintain consistent signal amplitudes and characteristics between the input and output of the instrumentation and general-purpose amplifiers. A schematic for the ADC circuit is shown below in *Figure 9*. In the middle of the schematic is the differential drive circuit, which takes the output of the low-noise amplifier (denoted by the SMA port symbol) and converts it to the differential ADC input. The schematic mainly uses nets (the arrow symbols) to minimize the use of wires, so it is difficult to see some of the connections, but the ADC is powered by the power supply circuits on top of the schematic and outputs to the digital output pins on the left side.



Figure 9: Schematic of the ADC and Differential Driving Circuit

**Stage 4: STM32F4 Microcontroller:** The MCU, an STM32F407, handles the synchronization of the ADC output, the reception of the ADC data, and the packaging of that data into neatly arranged messages that the ESP32 can receive and send over the air to the user's computer. The ARM Cortex  $M_4$  processor that this microcontroller is equipped with is a very capable device, running at nearly 200 MHz versus the typical 16 MHz that AVR-based boards run at, with a more comprehensive and cycle-efficient instruction set. It also contains a wide array of peripherals and features for development use, but our team is mainly interested in simply receiving parallel inputs, using the Direct Memory Access (DMA) module to automatically move inputs into memory, then writing SPI messages to the  $ESP_32$  as quickly as we receive the data. The  $STM_32$  will also output a clock signal to indicate to the ADC how fast it should send its parallel bits of digitized signal data for processing by the STM. See an example circuit for the MCU in *Figure* 10 *below*.



Figure 10: Minimal STM Circuit for Pin-Compatible F4 MCU

**Stage 5: ESP Wi-Fi Module:** For our wireless communication, we will be utilizing an  $ESP$ 32 with our  $STM$ 32 $F$ 4 Microcontroller. The microcontroller will package messages and provide them to the ESP32 which will then send them as a server in six-byte messages. Figure 11 below shows the physical Wi-Fi module that we will be adding to our device.



*Figure 11: ESP32 Wi-Fi Module*

With this module, a user will be able to see the device pop up on their laptop Wi-Fi setting and will be able to connect. The LabVIEW interface will provide the IP address and port of the device which will make the connection in the GUI. Once the device is connected to the laptop and GUI, messages can be read that the ESP32 is constantly sending over the server.

• **Stage 6: User Interface:** The GUI will be a very important part for the user experience. The goal for our user interface is to provide data to the user with minimal latency, provide a useful interface for data analysis, and allow the user to record data. LabVIEW will allow us to connect to the device using a Transmission Control Protocol for network communication. For this we will need to provide the IP address and port which we can set/ discover using the Arduino IDE ESP32 Library (this should only need to be done one time). Once the IP address is known and the port is set, we can configure a TCP block in LabVIEW. LabVIEW will also provide a graph for data and a data logging option to a text file, which are both capabilities of LabVIEW software.

Lastly, the flowchart and block diagram that visually depicts the process flow of the six stages of our device from start to finish is shown below in *Figure 12*.



*Figure 12: Block Diagram of the Process Flow (Split into Two Rows)* 

## <span id="page-32-0"></span>4.3.3 Functionality

Our device is intended to be used at the ISU biomedical imaging lab (BILab) with a Photoacoustic Tomography (PAT) system that conducts experiments on small animals. Reference *Figure* 13 for a visual depiction of the PAT system. The wDAQ will be used to capture high frequency (MHz range) signals, created from a device called a transducer that converts physical signals to electrical signals, and wirelessly transmit the data in real time to the users' computers. There will be two channels on the device: one to trigger and another for signal acquisition. The user can view the data through an application called LabVIEW with the support of an easy-to-connect Wi-Fi module. LabVIEW offers users the ability to completely control the information they wish to view. For instance, they will have the option to modify axis scales and select which window(s) they are viewing.

Upon successful completion of the first device, a batch of 10 to 20 copies of the device will be produced and connected to an array of transducers in a circular configuration within the rotating PAT system. The primary users of this device will be lab technicians and graduate students that are familiar with technical systems within the BILab. Although the primary user will have experience with sophisticated systems, the device will be designed to cater to users of all levels of experience and expertise.



*Figure 13: Visual demonstration of how the PAT system operates [2]* 

# <span id="page-32-1"></span>4.3.4 Areas of Concern and Development

Our most recent iteration of our device's design satisfies most user needs and requirements. The Low-Noise Amplifier & Filter (LNA), the Analog-to-Digital Converter (ADC), the STM32F411 microcontroller, the ESP32 Wi-Fi Module, and LabVIEW user interface have all been designed to an individually functional level so far. In addition, the PCBs for the LNA and ADC were designed, and we ordered PCBs to be soldered for these components. Once we have completed testing the hardware and software for each individual portion of our design, we are aiming to combine the individual components of the design in late April/early May to create a functional prototype, which will be tested and then revised in the Fall semester.

As we work on creating future iterations of the design and eventually our final product, we will want to be sure we are placing a focus on compact sizing, clean traces for the PCB, a strong wireless connection between the device and user software and meeting all user needs and requirements given in the project proposal. Our device relies on the  $STM<sub>32</sub>F<sub>411</sub>$ , ESP<sub>32</sub>, and GUI to communicate a lot of data quickly, so for this to work with minimum latency, our programming needs to be as efficient as possible. Our team will also need to test our device and interface to inspect its capabilities within different environments and ensure the data being presented is accurate.

The primary concerns our team has right now related to delivering a prototype and final product that addresses all requirements are that first of all, some of the traces in our PCBs are somewhat sloppy and messy, leading to certain PCB designs being overcrowded with wires and confusing connections when they potentially don't need to be, and the final design can be made cleaner. Additionally, the initial tests of the Wi-Fi module have indicated some unanticipated latency with the data transfer process, as well as some unexpected difficulties with connecting the device to Wi-Fi initially, which may or may not require further testing and steps to resolve. Overall, we are all slightly concerned about being able to fully design, order, and test a complete prototype for our device before the end of the semester in May, because we only have about a month to complete our work and combine our individual designs into one.

Our immediate plans for addressing these concerns and solving these problems is consistent communication and more frequent team meetings from now through the end of the Spring semester. We are facing issues with certain portions of the design not being completed in a timely manner, while others are being completed ahead of schedule, so the best way to resolve these discrepancies and ensure we are working at the same pace is by meeting and communicating more frequently. By sticking to this slightly more rigid schedule and committing to better communication for the rest of the semester, we can set ourselves up for success in completing the design and buildout of our first functional prototype by May.

#### <span id="page-33-0"></span>**4.4 TECHNOLOGY CONSIDERATIONS**

With our project's overall complexity, we have been required to use innovative technologies to accomplish our goals and requirements. The first technology we have worked with is a free to use program called EasyEDA. This is a program that allows its users to build circuit schematics from their wide range of libraries and export them to PCB layouts. EasyEDA also offers functions like auto-route to route traces in the board all while minimizing the distance and number of turns. EasyEDA also offers a unique way for teams to collaborate on projects through their fullonline version. This has allowed for everyone to work, analyze, and review on a subsystem. Once a project has been completed, EasyEDA offers easy to export bill-of-materials and files that make sourcing the parts and boards easier than ever. This paired with its built-in functions and libraries have saved countless hours of work.

Another main aspect of our design is chip selection because multiple portions of the project require chips to perform an action. The two main blocks of the project that require IC chips are the Low-Noise-Amplifier and ADC. Some considerations for the chip selection in the LNA are signal-to-noise-ratio (SNR), if the device requires unipolar or bipolar biasing, system gain, size, and cost. The most important of the criteria is SNR and biasing because it plays a direct role in the functionality of the device. As for the ADC, some technological considerations are resolution,

sampling rate, size, cost, and input. Zooming in further, our project requires an ADC with a differential input. So, another technological consideration comes into play because there are a few methods to establish a differential input. One of them being use of an instrumentation amplifier; the other being the use of a special transformer supplied by Texas Instruments. Both increase the overall complexity of the device, size, and cost but the aspect that separates the two is that a transformer operates poorly at high frequencies. Given that our project will operate in the MHz range this all but eliminates the possibility of a transformer.

For our wireless communication aspect, our team considered the options of Bluetooth or Wi-Fi. We had distinct needs of message size, connectivity range, and latency. We had researched to find two modules for each type of wireless communication that we considered to fit our constraints. Our device currently only needs a range of 10 meters, which made the HC-05 Bluetooth module a good option compared to the ESP32 Wi-Fi module which provided up to 100 meters of connectivity. The ESP32 allows much more of a range than we need but could potentially provide room for growth. Our main concern for the modules is the baud rate and the latency. By creating test stands, we could observe the reaction of our interface connection with the modules to discover how the latency would be affected by the amount of data being sent.

For the signal processing, our team considered two primary options. We have to target a sample rate on the order of tens of megahertz, and although an FPGA board provides the most outright performance, the programming overhead and actual cost of implementing this option makes it non-scalable and unrealistic, rendering a microcontroller of some kind the only viable type of solution to choose from. A combination of raw clock speed and instruction efficiency have to be considered when looking for a suitable microcontroller, so Arduino-like boards were out of the question. The ESP32, an Arduino compatible board, was considered for the speed of development and neat packaging that includes the Wi-Fi and data processing components in one place. While the raw clock speed is potentially double that of similarly priced options, the design of the peripherals crucial to our project were lacking in speed and features, and the instructions require significantly more CPU clock cycles for an equivalent program on many other platforms.

The STM32 is a widely used ARM Cortex microcontroller with a diverse range of features, variation in products for different applications, and simply better performance in the areas that we seek. The clock speed on even the most affordable options eclipses AVR options by tenfold in most cases. The power consumption is also lower than an ESP32 and even the lower power Arduino boards. Instruction-set wise, there are a larger number of types on an ARM CPU than with an AT Mega Arduino CPU, consuming just a single clock cycle to accomplish what would take between 2 and 4 cycles on an AVR-based chip. These things all mean that the ARM CPU can process and send data at a rate that meets our requirements for sample-rate, and by extension bandwidth & latency.

#### <span id="page-34-0"></span>4.5 DESIGN ANALYSIS

So far, our project is finalizing the design for a few of the project stages. Starting off with the low-noise amplifier  $(LNA)$  we were able to test a single rail IC chip called the MARS-6SM+ on a PCB board and test its characteristics. Our team was able to determine that with 2 of these ICs cascaded together and single 12-volt supply, we were able to get a gain of about 6odB. This prompted us to create circuit schematics and PCB layouts of our own using the MARS-6SM+ and a

combination of passive components to establish a bandwidth of 100kHz-2.2GHz. The team is currently waiting for the boards to be soldered so testing & evaluation can be conducted to determine if the design meets the requirements. The next stage we are in the midst of completing is the ADC. For our design, we are using a 12-bit ADC, ADC 12020. The chip has a differential input, so we have implemented an instrumentation amplifier, and a network of passive components to establish a differential input and drive the ADC. Similar to the LNA, its circuit schematic and PCB layout have been completed and the team is waiting for the device to be soldered so test and evaluation can be conducted. It is worth noting that the devices make use of 50-Ohm SMA connectors. This will allow all the signals to propagate from one stage of the device to the next and tests and evaluations are conducted.

Development on a completely bare-bones platform to maximize speed has its tradeoffs, but the benefits factor in more heavily when the scope of the microcontroller's tasks are reliant on just a few simple instructions executed at the upper edge of available speed. The program so far uses several dummy values for debugging purposes, but the peripheral modules on the Cortex  $M_4$  that are in use are configured to run as fast as possible, at minimum  $2.5$  times the frequency of the ADC's highest possible sample rate. The largest task is to configure the inputs and data buffers to minimize latency, and efficiently format/package incoming data in a way that uses as little CPU overhead as possible. All of this must happen reliably and be synchronized with only a small window for error. The next step will be to understand how to utilize the DMA module to increase program parallelism and further reduce processor cycles used.

Throughout the semester we have tested different wireless modules to learn their capabilities. To do this we created two test setups using a Wi-Fi module and a Bluetooth module programmed with an Arduino. These test setups allowed us to learn the capabilities and restrictions of the wireless connections which led us to choose an ESP32 Wi-Fi module for our device. We found that the module provided the least amount of latency, a further connection distance, and allowed us to transmit a large amount of data. We also tested both connected Bluetooth and Wi-Fi to LabVIEW and different methods of presenting the data we wanted to the user. Today, our team has made a test stand with a ESP32 Wi-Fi module and LabVIEW Interface that successfully communicates and presents data to the user. In the future, we want to work on this interface to improve the optimization of the LabVIEW program to faster process data and present it. We would also like an option in LabVIEW for the user to be able to record data to a text file. Currently, our interface has also been made for a developer which allows us to test factors such as delays, errors, message size, etc., in the future we will need to redesign and decide which features the user will actually need available.

# <span id="page-35-0"></span>5 Testing

#### <span id="page-35-1"></span>5.1 UNIT TESTING

The first stage of our device that requires testing is the LNA. Tests are conducted in a few manners. The first being virtual simulations using LTSpice and NI Multisim to get a high-level understanding of overall performance. The next test is conducted upon the fabrication of the first prototype. Using testbench equipment like Oscilloscope, wave generators, and multimeters experiments seek to validate virtual simulations. Further, data is collected on the devices' input frequency and amplitude, and the DC operating.

The second stage of the device that requires testing is the ADC. Following a similar procedure as the LNA a variety of designs are virtually simulated using LTspice and NI Multisim. Following this, the superior design is physically fabricated and physical tests are conducted. Using testbench equipment, tests using various inputs are done to see the digital outputs. The ADC also needs to be physically connected to the STM32 MCU, to validate that the configuration allows for the required output speed and data rate.

The third stage in the wireless DAQ is the STM32 microcontroller. Utilizing the  $STM_{32}F_{411}$  variant, our system must transform the parallel output from the ADC into a message that the ESP32 can send to the user's computer. To do this, we must write code to perform two main tasks. The program must continuously read 12 inputs first, and then send the status of those inputs as a number to the ESP module. The code must succeed in performing each of these things individually at a human-readable rate first to test functionality, and then simultaneously to provide the ESP32 with a realistic data rate. A separate function is to communicate with the ESP32 via SPI, but this type of communication protocol is used as an inbuilt function, so a simple visual confirmation of valid data will suffice for testing purposes.

The last portion of testing that is required is with the ESP32. Paired with an Arduino microcontroller, data is collected on temperature. The ESP32 then takes this data and transmits it via Wi-Fi to a remote laptop that has LabView. The test is done properly, the laptop will display the data in real time. This test simulates the exact tasks the ESP32 will perform when integrated into the whole system.

#### <span id="page-36-0"></span>5.2 INTERFACE TESTING

The main interface that constitutes our design is the graphical user interface (GUI), created in LabVIEW. This interface connects the device to software on a computer for analysis of signals. The interface provides an interface like a traditional oscilloscope showing a graph to the user of voltage and time. The interface also provides features to the user to record data and export it to a text file.

There are multiple factors we will need to test to analyze and improve our user interface. The first part of testing will be strongly geared toward the development sector. We need to ensure minimal latency between the signals and when they are displayed to the user and the data's accuracy. One way we will test this is by comparing the results of our device with traditional, reliable oscilloscopes. For our device to be successful, it will need to provide real-time data with nearly unnoticeable latency. The other part of our interface we will need to test is user satisfaction and reliability. We will need to run our device and interface for different periods of time to see that it is a reliable resource. Our team will also conduct testing with real-world users, such as our clients, to make sure that they are satisfied with the interface and its functionality.

#### <span id="page-36-1"></span>5.3 INTEGRATION TESTING

Due to the complexity of our project individual components are tested by themselves and then are tied together. On the hardware side, the LNA, ADC, Microcontroller, and ESP32 Wi-Fi module will need to be tested. The individual components all serve a critical role in our device and without one the other cannot occur. The LNA must sufficiently amplify and filter the input signal for the ADC to properly digitize it. The implementation amplifier must properly create a differential input for the ADC. The ADC must properly digitize that data with enough resolution that the data is arcuate and able to be interfaced with the STM32f411. The STM32 MCU executes the actions necessary for the ESP32 to transmit the ADC data. On the software side, the MCU must be correctly programmed across every necessary register address and provide a valid I/O configuration to integrate with the ADC, ESP, and battery components. The ESP32 and LabVIEW will need to communicate in serial to support proper communication. All things considered, these devices must properly be integrated together on both the hardware and software level for the device to function as necessary.

The general approach to this integration has come in the form of diving and conquering. The individual stages are tested separately to verify functionally and reduce large scale trouble shooting of a 100% tied together device. On the hardware side individual PCB boards are initially created. They are designed so that they can be tested individually but can also be tied to the other seperate PCB boards through the use of SMA cables. This critical test strategy has isolated problems to individual boards and supports integration. It also allows for hardware to be interfaced with software at any given time. The two test strategies for software were initially splitting the MCU and  $ESP<sub>32</sub>$ . Using a development board, we were able to design the code required to make the heart of the device function. This erased most of the hardware troubleshooting that came with a PCB layout of an MCU. In parallel to this test, the ESP32 was tested for its individual functionalities, and then connected to the MCU to observe their ability to interface together. The final integration test would be to put everything onto one PCB board and input a similar input signal. At the output would LabVIEW and the data can be timed to see if it's transmitted in real time, or if there are inaccuracies.

#### <span id="page-37-0"></span>5.4 SYSTEM TESTING

The wDAQ as a completed system has a few requirements to be considered a fully functional device: the device must be capable of taking an analog signal with an amplitude of approximately 1- $2 \text{ mV}$  and impedance of 50Ω as an input, then amplifying it by a factor of 1000 (volts per volt) to an output amplitude of approximately  $1-2$  V; the device must utilize an ADC with a bit resolution between 10 and 14 to digitize analog signals at a rate of one million samples per second; the device must be capable of manipulating signals with frequencies of up to 20 MHz, so its bandwidth should be at least this high (ideally up to five times as much) to ensure RF (radio frequency) signals are capable of being captured and analyzed; and the device must be able to be powered by a single 12volt DC power supply (achieved through a rechargeable battery). Lastly, the device must also be compatible with a graphical user interface, written in LabVIEW, and connected to said interface through a stable, reliable Wi-Fi connection.

In order to ensure the compliance of our device with each of these specifications and parameters, our team will need to perform system level testing, i.e., separate testing and analysis of the individual subsystems and circuits that comprise our overall system, as well as tests of the interfaces between the subsystems and the final integration of all subsystems into one to create the final product. As for individual unit tests, we will need to perform electrical tests on the low-noise amplifier, analog-to-digital converter (ADC), STM32 Microcontroller and Wi-Fi Module, and power supply circuits, to ensure that individual specifications are satisfied. With the low-noise amplifier, upon design and assembly of the circuit, we will need to test the circuit's performance across a range of input amplitudes, frequencies, and power supply voltages to ensure that the circuit can amplify a 1-2 mV signal, at any frequency between  $1$  kHz and 20 MHz, to an output of 1-2 V, without significant degradation of the signal quality. This testing has already been performed on initial prototype PCBs of our low-noise amplifier, which enabled us to conclude that we would achieve better performance and voltage gain characteristics by cascading two of our amplifier circuits together in series. With the ADC, we will need to verify that the circuitry surrounding it is capable of effectively creating a differential (double-ended) analog input from the single output voltage of our amplifier stage, and that the ADC chip we select is able to properly convert an analog

(continuous-amplitude, like a sinusoid) input signal to a digital (discrete-amplitude, like a square pulse) output signal, again, without attenuating or degrading the signal. With the power supply, we must ensure that the battery and associated circuitry we utilize can produce a steady 12-volt DC voltage, which can be achieved using a linear voltage regulator IC to maintain the voltage at a steady, constant value. Lastly, with our user interface, we will need to ensure that the software tools are relatively easy to use and understand, and that the interface can successfully display a signal from the device in a user window with adjustment tools.

Testing the interfaces between individual subsystems in our circuit is where the Wi-Fi connection between the device and the GUI will be tested. The interface will need to be completed to a working extent, such that it can acquire and display data from the device when it is connected; and preliminary tests will focus on establishing a successful Wi-Fi connection between the GUI and an ESP<sub>32</sub> Wi-Fi chip on a standard evaluation board. Once it is confirmed that a stable connection can be obtained for an extended period, and that the user interface is capable of reading and outputting data from sensors on the evaluation board, deeper research and design will be conducted to create the biasing circuitry surrounding the Wi-Fi chip that we will be utilizing in our design. Once the final circuit for the Wi-Fi module is designed, ordered, and assembled, interface testing will continue to ensure that the Wi-Fi chip is still able to successfully initiate and maintain a connection between our device and the user interface in LabVIEW.

Lastly, in the way of integration testing, we will need to compile the individual circuits and subsystems of our device such that they are electrically connected, capable of interfacing with one another, and continue to meet all specifications of the design as noted in the requirements and the initial project proposal (including size constraints). The final device will first be tested in its prototyping phases, so the device may initially occupy more space than the design specifies, and it may be tested using a benchtop power supply in an ISU lab rather than the battery (as the battery circuit will be one of the last aspects of our design to be incorporated). As the prototype is tested and results are analyzed to draw conclusions and understand changes that must be made, future iterations of the full design will emphasize minimizing the size of our circuit to meet constraints and successfully integrating the battery and battery management system into our circuit.

#### <span id="page-38-0"></span>5.5 REGRESSION TESTING

As we progress with the design and implementation of our project, we may make decisions based on test results, team discussions, and client discussions, that lead us to alter our design to improve the performance and/or characteristics of our device. If we decide to implement such changes, it is critical for our team to ensure that they do not interfere with the existing functionality of the device, negatively alter or degrade the performance and signal characteristics of our device or cause the device to no longer meet certain specifications from the project proposal.

The critical features that have been implemented which we need to ensure we do not break through changes to our design are all driven by the specifications and requirements of the design: we must not alter the voltage and gain characteristics of the amplifier that we have established (which currently satisfy the proposed requirements), nor the bandwidth of the signals that our circuit is capable of manipulating (because the circuit will be used primarily with radio-frequency signals). We also must take care to ensure that the parts of the device that interface together (mainly the Wi-Fi connection between the device and the user interface) are not upset by future

changes or iterations of our design, as the device will be useless if the user interface is not able to connect to the device to analyze data.

#### <span id="page-39-0"></span>5.6 ACCEPTANCE TESTING

As we progress through continued testing and future iterations and development of our design, we will need to demonstrate to the parties interested in our design that our design meets the requirements (functional and non-functional) initially stipulated in the project proposal, or that the device otherwise satisfies any requirements or specifications that have been revised or approved for addition to the design since the initial proposal. This process is referred to as "acceptance testing" and will primarily involve our client, as well as ultimately our faculty advisor and potentially a panel of faculty or industry professionals reviewing our design.

Acceptance testing will follow a similar protocol to system testing in that we will be testing the performance of individual subsystems of our design in addition to the performance and effectiveness of interfaces and connections between our subsystems and the top-level system. Because many of the specifications of the design are associated with specific subsystems, testing the design to ensure compliance with functional requirements will entail testing some of these subsystems individually. For instance, the low-noise amplifier will need to be tested to demonstrate that the voltage gain and bandwidth requirements for the device are being met, while the battery circuit and any voltage regulation and conversion circuitry associated with it (i.e., linear voltage regulators and DC-DC step down buck converters) will need to be tested to verify that a steady DC power supply of 12 volts is present across the circuit, with voltage being stepped down properly from the single voltage source for parts of the circuit that require a lower supply voltage (e.g., the ADC circuit, which requires a voltage of  $\frac{1}{5}$  V DC). The graphical user interface and Wi-Fi connection should be straightforward to test once they have been fully designed and built out, because testing these components will simply require operating the user interface in LabVIEW, connecting to the data acquisition device via a specific Wi-Fi network, and successfully acquiring and displaying data for user analysis in the program. Throughout this process, our client will be heavily involved and engaged in troubleshooting and problem solving.

#### <span id="page-39-1"></span>5.7 RESULTS

Tests up to this point have yielded a mix of positive and negative results, but most results have signified that our team is on the right track with our design and making successful steps toward satisfying all the design requirements.

On the electrical front, we have performed numerous tests on the low-noise amplifier (LNA), as well as some preliminary tests with the ADC circuit, to ensure compliance with our specifications. Our latest revision of the LNA circuit has proved successful in terms of producing a signal with an amplitude of nearly 2 volts (peak-to-peak) from an input of  $2 \text{ mV}$  (peak-to-peak), and we have successfully shown that our amplifier can produce a similar level of signal gain at nearly any frequency across the bandwidth that our circuit will need to support. *Figures* 14, 15, and 16 below show test results on our LNA circuit at three different frequencies across our bandwidth: 100 kHz, 1 MHz, and 10 MHz, respectively. Each test utilized a 12-volt benchtop DC power supply for the voltage source.



*Figures* 14, 15, and 16: Output Waveforms for the Low-Noise Amplifier at Frequencies of 100 kHz, 1 *MHz, and 10 MHz (Left to Right)* 

Simulations of our design for the ADC circuit have yielded promising results, but tests of the physical circuit have yet to take place to ensure that the circuit is able to convert a single-ended analog signal to a differential input to the converter, as well as to ensure that the ADC can produce a digital output capable of interfacing with the GPIO (general-purpose input-output) pins on the STM<sub>32</sub> Microcontroller and its associated circuitry.

Lastly, with the user interface, a significant portion of the code has already been developed, and recent tests have allowed us to continuously plot serial voltage data points with respect to time on a graph with titles, axis labels, and increment markings. *Figure 17* below shows a successful serial plot of voltage sensor data from the evaluation circuit for the Wi-Fi chip. The ability to plot serial voltage data from a circuit in the LabVIEW interface required a successful Wi-Fi connection between LabVIEW and the test circuit, which was successfully established and maintained for an extended period during these tests.



Figure 17: Plot of Voltage Values Over Time Obtained from Data in LabVIEW

Overall, while tests are still being conducted on a regular basis as our team progresses through successive iterations of our design, the tests and results we have acquired up to this point have indicated that our design already satisfies several of the specifications and requirements of the project proposal, and that continued progress, changes, and testing will ensure that all requirements and specifications are met and that individual aspects of the design can be successfully synthesized to create a functional data acquisition tool.

# <span id="page-41-0"></span>6 Implementation

While the bulk of the implementation for our project is intended to occur over the next semester, in  $EE/CprE/SE/CybE$  492, a significant portion of implementation and physical assembly has already occurred during our work in  $EE/CprE/SE/CybE$  491. Namely, we have completed the first few revisions of our design for the low-noise amplifier (LNA) and ADC circuits and have already assembled prototype PCBs for these subsystems.

With the ADC, our circuit has yielded questionable results that have led us to partially reconsider our design for the circuit and choice of device, but for the LNA, we have soldered multiple test PCBs for the circuit and have performed a series of tests on the circuit at a range of frequencies, input voltage amplitudes, and power supplies. Because these tests have shown us that our amplifier can meet the performance requirements of our design needs, we are relatively confident that we would like to implement this design in our final deliverable. We have also implemented a primary version of our graphical user interface that can successfully read and plot serial data from an evaluation board, which will be able to be connected to our Wi-Fi and microcontroller circuit once it has been implemented.

Moving forward, the primary plan for the further implementation of our proposed design will involve a standard rinse-and-repeat process of design, prototype testing  $\&$  analysis, revisions  $\&$ troubleshooting, and testing & implementation of said revisions. We will mainly be working separately on the individual subsystems to implement them one at a time, as we have done throughout the design  $&$  testing phases (i.e. testing and implementing the low-noise amplifier, ADC circuit, microcontroller & Wi-Fi module and circuitry, and graphical user interface), before synthesizing and interfacing the individual subsystems together to implement the top-level design.

# <span id="page-41-1"></span>7 Professional Responsibility

# <span id="page-41-2"></span>**7.1 AREAS OF RESPONSIBILITY**

*Table* 7 below shows the similarities and differences between the IEEE and NSPE Codes of Ethics based on IEEE and NSPE publications  $[7]$  and  $[8]$ .





Table 7: Similarities and Differences Between IEEE's and NSPE's Codes of Ethics [7] [8]

#### <span id="page-43-0"></span>7.2 PROJECT SPECIFIC PROFESSIONAL RESPONSIBILITY AREAS

#### Work competence: High

The technical ability of the team and each individual team member is suitable for this type of project, and each team member has adapted their knowledge and expanded their skillset. Together, our team is in the initial stages of full system integration and has not exercised a full spectrum of teamworking skills at this point.

Financial responsibility: Low

Our team has not been performing to the highest standard. When procuring components, we have cut counters to save time, making purchasing. This equated to mismanagement of funds. Long term our project can cut costs of the university in procurement of expensive imaging equipment.

Communication honesty: High

Our communication could use some improvement. In general, we have exercised a high degree of communication honesty, but as documentation increases our ability to communicate everything can stagnate. Taking a more proactive approach would move our communication honesty from moderate to excellent.

Health, safety, and well-being: High

The risk of injury and damage to people or property is low for a project like this. The minimal requirements for safety, such as simple PPE and fundamental knowledge of electrical safety are very well understood and followed. 

Property ownership: Medium

Our team has employed a mix of self-developed solutions and free-to-use segments of code and physical designs. There are several items that make the most sense to buy and alter, but copyright infringement is not typically an issue with such components or devices. However, explicit permission may be required depending on how the remaining software is implemented.

#### Sustainability: Medium

As of now our application of sustainability is low because we are still in the test and evaluation phase. In the long term, this project doesn't seem to indicate that it will impact environmental and global resources.

Social responsibility: Low

Regarding social responsibility, the product isn't applicable to a wider community/society, but the biological community involved with cancer research at Iowa State will greatly benefit from the work being conducted to improve mobility and reliability of data acquisition.

#### *Table 8: Project-Specific Areas of Professional Responsibility*

#### <span id="page-43-1"></span>7.3 MOST APPLICABLE PROFESSIONAL RESPONSIBILITY AREA

The most applicable area of professional responsibility to our team's design is property ownership. It is always important to give credit where credit is due and avoid claiming designs, work, or ideas that are the intellectual or physical property of others, whether said property is protected by a copyright or not. Throughout our design, we have incorporated a significant number of existing designs and ideas into our project, or at least drawn inspiration from said designs or ideas, and it is highly important that when we complete our design and potentially publish a research article about our design, we thoroughly credit all resources used throughout our work.

# <span id="page-44-0"></span>8 Closing Material

#### <span id="page-44-1"></span>8.1 DISCUSSION

The final goal of our project is to physically replace a traditional oscilloscope from being needed with a lab imaging device. Once we have processed all over our testing, revised our design, and retested with successful results we will implement our device into a lab setting. If our device replaces an oscilloscopes functionality to our client's satisfaction, we can consider our project goal achieved.

#### <span id="page-44-2"></span>8.2 CONCLUSION

Currently, the project is sitting in the test and validation stage. Throughout the semester, we have compiled research on similar devices and potential design strategies. Following this, we have been able to simulate hardware that might play a role in making our product stand out. We have been able to decide on components, implement them on PCB boards, and integrate them with minimally functional software.

Our main goals have been to create a system that takes a signal, amplifies, filters, digitizes, and transmits it to a computer. The device will need to be constructed on a single board, minimally sized, and promote a mobile work style. Ease of user interface is another key goal of our device. These goals tend to be constrained by economic, time, and equipment barriers. As we move forward with successive iterations of our design, we will need to be increasingly conscious of these constraints and ensure we are completing our work and implementing our design in a costeffective, timely, and resourceful manner, while also being aware of the environmental impacts of our design and the potential effects of our design on different user groups that may arise.

#### <span id="page-44-3"></span>8.3 REFERENCES

- [1] Ikalogic, "IKAscope Portable Oscilloscope," Ikalogic, Accessed: April 16, 2024. Available: <https://www.ikalogic.com/ikascope-portable-oscilloscope/>
- $[2]$  Digilent Inc., "Analog Discovery 3," Digilent, Accessed: April 16, 2024. Available: <https://digilent.com/shop/analog-discovery-3/>
- [3] Pokit Innovations Pty Ltd, "Pokit Pro," Pokit Innovations, Accessed: April 16, 2024. Available: https://shop.pokitmeter.com/products/pokit-pro
- [4] Dewesoft. (2022, September 20). What is an ADC Converter? Dewesoft. <https://dewesoft.com/blog/what-is-adc-converter>
- [5] T. Vu, D. Razansky, and J. Yao, "Listening to tissues with new light: recent technological advances in photoacoustic imaging," J. Opt., vol. 21, no. 11, p. 113001, 2019. [Online]. Available: https://iopscience.iop.org/article/10.1088/2040-8986/ab3b1a
- [6] "Cortex M-4 Technical Reference Manual." *Documentation – Arm Developer*, ARM Limited, 2010, developer.arm.com/documentation/ddi0439/b/CHDDIGAC
- [7] J. M. Pearce and E. Z. Horsch, "Contextualizing Professionalism in Capstone Projects Using the IDEALS Professional Responsibility Assessment," International Journal of Engineering Education, vol. 28, no. 2, pp. 416-424, 2012.
- [8] IEEE, "IEEE Policies," IEEE, [Online]. Available: https://www.ieee.org/about/corporate/governance/p7-8.html. [Accessed: April 16, 2024].

## <span id="page-45-0"></span>8.4 APPENDICES

<span id="page-45-1"></span>Appendix 1.2: User Personas, Empathy Maps, and Journey Maps

# 9 Team

## 9.1 TEAM MEMBERS

- **Adam Shoberg:** Electrical Engineer
- **•** Henry Chamberlain: Electrical Engineer
- Lisa Tordai: Software Engineer
- **Vaughn Miller:** Computer Engineer

# 9.2 REQUIRED SKILL SETS FOR YOUR PROJECT

• PCB Design

- Circuit Design and Simulation
- 3D Modeling
- Software Development
- Soldering
- Embedded Systems
- C (Programming Language)
- Graphical User Interfacing

#### <span id="page-46-0"></span>9.3 SKILL SETS COVERED BY THE TEAM

- **PCB Design:** Henry Chamberlain, Adam Shoberg
- **Circuit Design and Simulation:** Adam Shoberg, Henry Chamberlain
- **3D Modeling and Printing:** Henry Chamberlain, Adam Shoberg, Lisa Tordai
- **Software Development:** Lisa Tordai, Vaughn Miller
- Soldering: Henry Chamberlain, Lisa Tordai, Vaughn Miller, Adam Shoberg
- Embedded Systems: Vaughn Miller, Henry Chamberlain, Adam Shoberg, Lisa Tordai
- **C** (Programming): Lisa Tordai, Vaughn Miller, Henry Chamberlain, Adam Shoberg
- **Graphical User Interface:** Lisa Tordai, Vaughn Miller

#### <span id="page-46-1"></span>9.4 PROJECT MANAGEMENT STYLE ADOPTED BY THE TEAM

For our senior design project, our team adapted Agile methodologies to navigate project management. We held regular weekly meetings where we assessed progress, discussed pending issues, and allocated tasks for the upcoming week. At each meeting our team aligned with a oneweek sprint cycle, setting specific goals and deliverables for each individual to ensure clarity and accountability within the team. Utilizing the Agile framework allowed us to adapt to conflicting issues and prioritize tasks. leading to a more efficient project workflow.

#### <span id="page-46-2"></span>9.5 INITIAL PROJECT MANAGEMENT ROLES

- **Adam Shoberg [EE]:** Circuit Design & Simulation, PCB Design, Team Communications
- **Henry Chamberlain** [EE] PCB Design & Assembly, Parts Acquisition, Documentation
- Lisa Tordai [SE] Software Development, Wireless Data Sharing, Team Website
- **Vaughn Miller [CprE]** Computer Engineering, Microcontroller Programming

#### <span id="page-46-3"></span>9.6 Team Contract

#### **Team Members:**



 $3)$  Henry Chamberlain  $4)$  Vaughn Miller

#### **Team Procedures**

- 1. Day, time, and location for regular team meetings: Wednesday, 1-2PM, SICTR Conference Room, in-person
- 2. Preferred method of communication updates, reminders, issues, and scheduling: Phone, Microsoft Teams, Outlook, Snapchat
- 3. Decision-making policy: Pro/con with final consensus
- 4. Procedures for recordkeeping: Google Docs (shared responsibility)

## **Participation Expectations**

- 1. Expected individual attendance, punctuality, and participation at all team meetings: Individuals will attend the meetings Bi-weekly and inform group members of any conflicts with attendance.
- 2. Expected level of responsibility for fulfilling team assignments, timelines, and deadlines: Setting schedules and assigning responsibilities to complete items before deadlines
- 3. Expected level of communication with other team members: Individuals should all be communicative via group chat or in-person communication about the status of their work and if they are expected to miss any meetings or deadlines
- 4. Expected level of commitment to team decisions and tasks: All team members should be actively involved in decisions and completing tasks.

# **Leadership**

- 1. Leadership roles for each team member:
	- a. **Henry Chamberlain:** Soldering, 3D modeling/printing, help with GUI, data collection, parts ordering and bills of materials, reporting and presentation
	- b. **Adam Shoberg:** PCB design and Testing, 3D Modeling, source parts and equipment, solder. Client Interaction.
	- c. Lisa Tordai: Software development: GUI, Database, testing software with hardware, documentation, and presentation.
	- d. Vaughn Miller: Firmware development and testing, Documentation, part specification, prototyping
- 2. Strategies for supporting and guiding the work of all team members: Planning of work/schedule, biweekly meetings with individual and group updates
- 3. Strategies for recognizing the contributions of all team members: Updating the faculty advisor and client frequently with work progress updates and individual members' contributions to the project.

# **Collaboration and Inclusion**

- 1. Skills, expertise, and unique perspectives each team member brings to the team:
	- a. Lisa Tordai: Software development, experience with LabView, MATLAB, and Python for GUI, experience with SQL and MongoDB to setup database, technical communication skills for reports and presentations
	- b. **Adam Shoberg:** Analog Circuits, Simulations (e.g. LTSpice, Cadence), Soldering, C Programming, Digital Circuits, Test Bench Equipment (Oscilloscope, Waveform Generators, Multimeters.)
	- c. **Henry Chamberlain:** Analog and digital IC analysis and simulation, surfacemount soldering, embedded systems fundamentals, C programming, creation of GUI in Python, lab bench equipment (e.g. oscilloscopes, waveform generators)
	- d. Vaughn Miller: C programming, microcontroller programming/embedded systems, Python, Java, Lab equipment, MATLAB, Simulink, CAN Bus, Soldering, Signal analysis
- 2. Strategies for encouraging and support contributions and ideas from all team members: Keeping an open mind to other's ideas and probing each other's thoughts on how to tackle the wide range of topics and problems this project contains will be a big part of our support network. This will include praise for good ideas and encouragement when things don't go as expected.
- 3. Procedures for identifying and resolving collaboration or inclusion issues: Our team will always encourage a collaborative and inclusive environment. Should any certain member have concerns about being held back from contributing and learning as much as they are capable of, they are encouraged to voice those concerns during team meetings or via group conversations on Snapchat.

#### **Goal Setting, Planning, and Execution**

- 1. Team goals for this semester: (copied from project proposal form)
	- a. **Project Planning and Design:** A comprehensive project plan outlining the tasks, milestones, and timeline. The design of the wDAQ system, including the selection of Wi-Fi/Bluetooth protocols and the specifications of the DAQ, should be finalized.
	- b. **PCB Design:** Complete the PCB design and SMT component assembly following the design constraints and technical specifications.
	- c. **3D Modeling:** Design and simulate the Electromagnetic (EM) shielding and casing of the system, followed by 3D printing.
- 2. Strategies for planning and assigning individual and teamwork:
	- a. Individual assignments and group tasks will be given during weekly team meetings. The goal is that individual work will be geared toward each team member's major and experience, i.e., software-related work will be more heavily delegated to SE/CprE members, while hardware and testing-related work may be assigned more heavily to the EE members.
	- b. Should a certain member want to work on something that someone else has been assigned, they are free to request to work on the parts of the project they prefer.
- 3. Strategies for keeping on task:
	- a. Team members are encouraged to stay off their phones and be as focused as possible during team meetings, client meetings, and faculty advisor meetings. When working on a project, individually or as a group, students should try to avoid outside distractions as much as possible.
	- b. The team should formulate a calendar or general agenda for checkpoints and tasks within the project to ensure everyone is staying on task and getting their work done in a timely manner.

#### **Consequences for Not Adhering to Team Contract**

- 1. How will you handle infractions of any of the obligations of this team contract? We will implement a liberal discipline policy. If the infraction is the group members first, we will decide as a team the situation, what needs to change, and how we can help the group members correct their behavior.
- 2. What will your team do if the infractions continue? If the infractions continue to arise and continued delegation is futile, we may seek outside help from the class professor, team coordinator or our contact.

\*

- a) I participated in formulating the standards, roles, and procedures as stated in this contract.
- b) I understand that I am obligated to abide by these terms and conditions.
- c) I understand that if I do not abide by these terms and conditions, I will suffer the consequences as stated in this contract.

